WHAT IS CLAIMED IS:

1. An integrated circuit device comprising:

a microelectronic substrate;

a dielectric layer on the substrate;

a conductive contact plug extending through an opening in the dielectric layer to contact the substrate and including a widened pad portion extending onto the dielectric layer adjacent the opening;

an ohmic pattern on the pad portion of the plug;

a barrier pattern on the ohmic pattern;

a concave first capacitor electrode disposed on the barrier pattern and defining a cavity opening away from the substrate;

a capacitor dielectric layer conforming to a surface of the first capacitor electrode; and

a second capacitor electrode disposed on the capacitor dielectric layer opposite the first capacitor electrode.

2. A device according to Claim 1, wherein sidewalls of the ohmic pattern, the barrier pattern and the pad portion of the contact plug are substantially coplanar.

3. A device according to Claim 2, comprising an etch stopper layer conforming to at least sidewalls of the ohmic pattern, the barrier pattern and the pad portion of the contact plug.

4. A device according to Claim 3, wherein the etch stopper layer also overlies a top surface of the barrier pattern.

5. A device according to Claim 3, wherein the etch stopper layer comprises a dielectric material having an etch selectivity with respect to at least material of a group including Hydrogen Silsesquioxane (HSQ), Boron Phosphorus Silicate Glass (BPSG), High density plasma (HDP) oxide, plasma enhanced tetraethyl orthosilicate (PETEOS), Undoped Silicate Glass (USG), Phosphorus Silicate Glass (PSG), plasma-enhanced (PE)-SiH_4 and aluminum oxide (Al_2O_3).

6. A device according to Claim 5, wherein the etch stopper layer comprises at least one material from a group including silicon nitride (Si_3N_4) and tantalum oxide (Ta_2O_5).

7. A device according to Claim 1, wherein the contact plug comprises polysilicon.

8. A device according to Claim 1, wherein the ohmic pattern comprises titanium silicide ($TiSi_X$).

9. A device according to Claim 1, wherein the barrier pattern comprises at least one material from a group including titanium nitride (TiN), tantalum nitride (TaN), tantalum aluminum nitride (TaAlN) and titanium aluminum nitride (TiAlN).

10. A device according to Claim 1, wherein the first electrode and the second electrode each comprise at least one material from a group including titanium nitride (TiN), tantalum nitride (TaN), tungsten nitride (WN), ruthenium (Ru), platinum (Pt), iridium (Ir), osmium (Os), rhodium (Rh), cobalt (Co) and nickel (Ni).

11. A device according to Claim 1, further comprising a metal etch stopper pattern interposed between the first capacitor electrode and the barrier pattern.

12. A device according to Claim 1, further comprising a support layer disposed on the dielectric layer and laterally abutting a base of the concave first capacitor electrode.

13. An integrated circuit device comprising:

a microelectronic substrate;

a dielectric layer on the substrate;

a conductive contact plug extending through an opening in the dielectric layer to contact the substrate and including a widened pad portion extending onto the dielectric layer adjacent the opening;

stacked ohmic and barrier patterns disposed on the pad portion of the plug and having sidewalls substantially coplanar with a sidewall of the pad portion;

a first capacitor electrode disposed on the barrier pattern;

a capacitor dielectric layer on the first capacitor electrode; and

a second capacitor electrode on the capacitor dielectric layer opposite the first capacitor electrode.

14. A device according to Claim 13, further comprising an etch stopper layer conforming to at least the sidewalls of the ohmic pattern, the barrier pattern and the pad portion of the contact plug.

15. A device according to Claim 14, wherein the etch stopper layer also overlies a portion of the barrier pattern.

16. A device according to Claim 14, wherein the etch stopper layer comprises a dielectric material having an etch selectivity with respect to at least one material from a group including Hydrogen Silsesquioxane (HSQ), Boron Phosphorus Silicate Glass (BPSG), High density plasma (HDP) oxide, plasma enhanced tetraethyl orthosilicate (PETEOS), Undoped Silicate Glass (USG), Phosphorus Silicate Glass (PSG), plasma-enhanced (PE)-SiH_4 and aluminum oxide (Al_2O_3).

17. A device according to Claim 16, wherein the etch stopper layer comprises at least one material from a group including silicon nitride (Si_3N_4) and tantalum oxide (Ta_2O_5).

18. A device according to Claim 13, wherein the contact plug comprises polysilicon.

19. A device according to Claim 13, wherein the ohmic pattern comprises titanium silicide ($TiSi_X$).

20. A device according to Claim 13, wherein the barrier pattern comprises at least one material from a group including titanium nitride (TiN), tantalum nitride (TaN), tantalum aluminum nitride (TaAlN) and titanium aluminum nitride (TiAlN).

21. A device according to Claim 13, wherein the first electrode and the second electrode each comprise at least one material from a group including titanium nitride (TiN), tantalum nitride (TaN), tungsten nitride (WN), ruthenium (Ru), platinum (Pt), iridium (Ir), osmium (Os), rhodium (Rh), cobalt (Co) and nickel (Ni).

22. A device according to Claim 13, further comprising a metal etch stopper pattern interposed between the first capacitor electrode and the barrier pattern.

23. A method of forming an integrated circuit capacitor, the method comprising:

forming a dielectric layer on a substrate;

forming a conductive contact plug extending through an opening in the dielectric layer to contact the substrate and including a widened pad portion extending onto the dielectric layer adjacent the opening and an ohmic pattern and a barrier pattern on the pad portion of the plug;

forming a concave first capacitor electrode on the barrier pattern and defining a cavity opening away from the substrate;

forming a capacitor dielectric layer conforming to a surface of the first capacitor electrode; and

forming a second capacitor electrode on the capacitor dielectric layer opposite the first capacitor electrode.

24. A method according to Claim 23, wherein forming a conductive contact plug extending through an opening in the dielectric layer to contact the substrate and including a widened pad portion extending onto the dielectric layer adjacent the opening and an ohmic pattern and a barrier pattern on the pad portion of the plug comprises:

forming the opening in the dielectric layer;

forming a conductive layer on the dielectric layer and in the opening;

forming an ohmic layer on the conductive layer;

forming a barrier layer on the ohmic layer;

forming a metal etch stopper layer on the barrier layer;

forming a mask on the metal etch stopper layer; and

patterning the metal etch stopper layer, the barrier layer, the ohmic layer and the conductive layer using the mask to form the conductive contact plug, the ohmic pattern on the pad portion of the contact plug, the barrier pattern on the ohmic pattern, and a metal etch stopper pattern on the barrier pattern.

25. A method according to Claim 24, wherein the conductive layer comprises polysilicon, wherein the ohmic layer comprises titanium silicide ($TiSi_X$), and wherein the barrier layer comprises at least one material from a group including titanium nitride (TiN), tantalum nitride (TaN), tantalum aluminum nitride (TaAlN) and titanium aluminum nitride (TiAlN).

26. A method according to Claim 24, wherein forming a concave first capacitor electrode comprises:

forming an etch stopper layer conforming to the metal etch stopper pattern, the barrier pattern, the ohmic pattern and the pad portion of the contact plug;

forming a mold layer on the etch stopper layer;

etching the mold layer to form an opening therein using the etch stopper layer as an etching stopper;

extending the opening through the etch stopper layer by etching the exposed portion of the etch stopper layer using the metal etch stopper pattern as an etching stopper;

forming a conductive layer on the mold layer and conforming to a sidewall of the opening through the mold layer and the etch stopper layer and the exposed portion of the metal etch stopper pattern; and

planarizing to form the first capacitor electrode.

27. A method according to Claim 26, wherein the conductive layer comprises at least one material from a group including titanium nitride (TiN), tantalum nitride (TaN), tungsten nitride (WN), ruthenium (Ru), platinum (Pt), iridium (Ir), osmium (Os), rhodium (Rh), cobalt (Co) and nickel (Ni).

28. A method according to Claim 26, wherein the mold layer comprises at least one material from a group including Hydrogen Silsesquioxane (HSQ), Boron Phosphorus Silicate Glass (BPSG), High density plasma (HDP) oxide, plasma

enhanced tetraethyl orthosilicate (PETEOS), Undoped Silicate Glass (USG), Phosphorus Silicate Glass (PSG), plasma-enhanced (PE)-SiH_4 and aluminum oxide (Al_2O_3), wherein the etch stopper layer comprises at least one material from group including silicon nitride (Si_3N_4) and tantalum oxide (Ta_2O_5), and wherein the metal etch stopper layer comprises at least one material from a group including tungsten (W), aluminum (Al), copper (Cu), titanium nitride (TiN), tantalum nitride (TaN), tungsten nitride (WN), ruthenium (Ru), platinum (Pt), iridium (Ir), osmium (Os), rhodium (Rh), cobalt (Co) and nickel (Ni).

29. A method according to Claim 23, further comprising forming a support layer on the dielectric layer and laterally abutting a base of the concave first capacitor electrode.

30. A method of forming an integrated circuit capacitor, the method comprising:

forming a dielectric layer on a substrate;

forming a conductive contact plug extending through an opening in the dielectric layer to contact the substrate and including a widened pad portion extending onto the dielectric layer adjacent the opening and stacked ohmic and barrier patterns disposed on the pad portion of the plug and having sidewalls substantially coplanar with a sidewall of the pad portion;

forming a first capacitor electrode on the barrier pattern;

forming a capacitor dielectric layer on the first capacitor electrode; and

forming a second capacitor electrode on the capacitor dielectric layer opposite the first capacitor electrode.

31. A method according to Claim 30, wherein forming a conductive contact plug extending through an opening in the dielectric layer to contact the substrate and including a widened pad portion extending onto the dielectric layer adjacent the opening and stacked ohmic and barrier patterns disposed on the pad portion of the plug and having sidewalls substantially coplanar with a sidewall of the pad portion comprises:

forming an opening in the dielectric layer;

forming a conductive layer on the dielectric layer and in the opening;

forming an ohmic layer on the conductive layer;

forming a barrier layer on the ohmic layer;

forming a metal etch stopper layer on the barrier layer;

forming a mask on the metal etch stopper layer; and

patterning the metal etch stopper layer, the barrier layer, the ohmic layer and the conductive layer using the mask to form the conductive contact plug, the ohmic pattern on the pad portion of the contact plug, the barrier pattern on the ohmic pattern, and a metal etch stopper pattern on the barrier pattern.

32. A method according to Claim 31, wherein the conductive layer comprises polysilicon, wherein the ohmic layer comprises titanium silicide ($TiSi_X$), and wherein the barrier layer comprises at least one material from a group including titanium nitride (TiN), tantalum nitride (TaN), tantalum aluminum nitride (TaAlN) and titanium aluminum nitride (TiAlN).

33. A method according to Claim 31, wherein forming a first capacitor electrode comprises:

forming an etch stopper layer conforming to the metal etch stopper pattern, the barrier pattern, the ohmic pattern and the pad portion of the contact plug;

forming a mold layer on the etch stopper layer;

etching the mold layer to form an opening therein using the etch stopper layer as an etching stopper;

extending the opening through the etch stopper layer by etching the exposed portion of the etch stopper layer using the metal etch stopper pattern as an etching stopper;

forming a conductive layer on the mold layer and conforming to a sidewall of the opening through the mold layer and the etch stopper layer and the exposed portion of the metal etch stopper pattern; and

planarizing to form the first capacitor electrode.

34. A method according to Claim 33, wherein the conductive layer comprises at least one material from a group including titanium nitride (TiN), tantalum nitride (TaN), tungsten nitride (WN), ruthenium (Ru), platinum (Pt), iridium (Ir), osmium (Os), rhodium (Rh), cobalt (Co) and nickel (Ni).

35. A method according to Claim 33, wherein the mold layer comprises at least one material from a group including of Hydrogen Silsesquioxane (HSQ), Boron Phosphorus Silicate Glass (BPSG), High density plasma (HDP) oxide, plasma enhanced tetraethyl orthosilicate (PETEOS), Undoped Silicate Glass (USG), Phosphorus Silicate Glass (PSG), plasma-enhanced (PE)-SiH_4 and aluminum oxide (Al_2O_3), wherein the etch stopper layer comprises at least one material from a group including silicon nitride (Si_3N_4) and tantalum oxide (Ta_2O_5), and wherein the metal etch stopper layer comprises at least one material from a group including tungsten (W), aluminum (Al), copper (Cu), titanium nitride (TiN), tantalum nitride (TaN), tungsten nitride (WN), ruthenium (Ru), platinum (Pt), iridium (Ir), osmium (Os), rhodium (Rh), cobalt (Co) and nickel (Ni).